**EE 465 Lab Report**

*Lab 1 – Function Design and Simulation*

Written by: Anh Q. Ho

Lab Section – Monday 04:10pm

Abstract

This is a warm-up lab, to refresh students the old materials from EE 230 and 330 with CPrE 281 verilog.

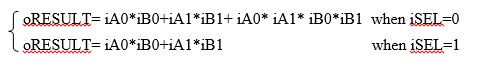
Introduction

This lab is created to model the Verilog coding of a mathematical function circuit and Verilog function simulation with ModelSim. This lab also use to refresh the topics from previous classes such as CPrE 281 (Verilog) and most importantly EE 330.

Topics:

1. Verilog Coding
2. Test bench construction
3. Function simulation

The target mathematical function use for this lab is:



where signals (i) are inputs and (o) for outputs.

The inputs and outputs are defined below.

iCLK – input clock signal 50MHz

iRST\_N – input reset signal, active low

iA0, iA1, iB0, iB1 – 8 bit binary unsigned integer input signals

iSEL – input selection signal

oRESULT – 17-bit binary unsigned integer output signal

results & Discussion

The table below shows the calculation of each step that are changed during the test bench

Table - Calculation of each step of the simulation.



Below is the Verilog code, test bench and simulation of the lab.

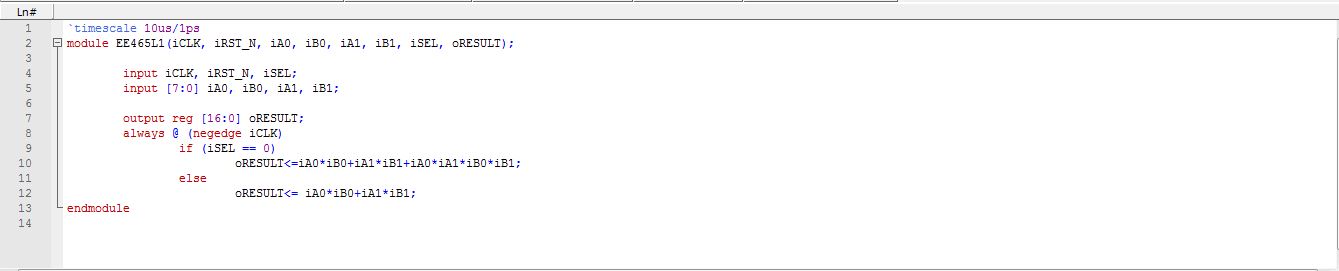


Figure - Verilog Coding.

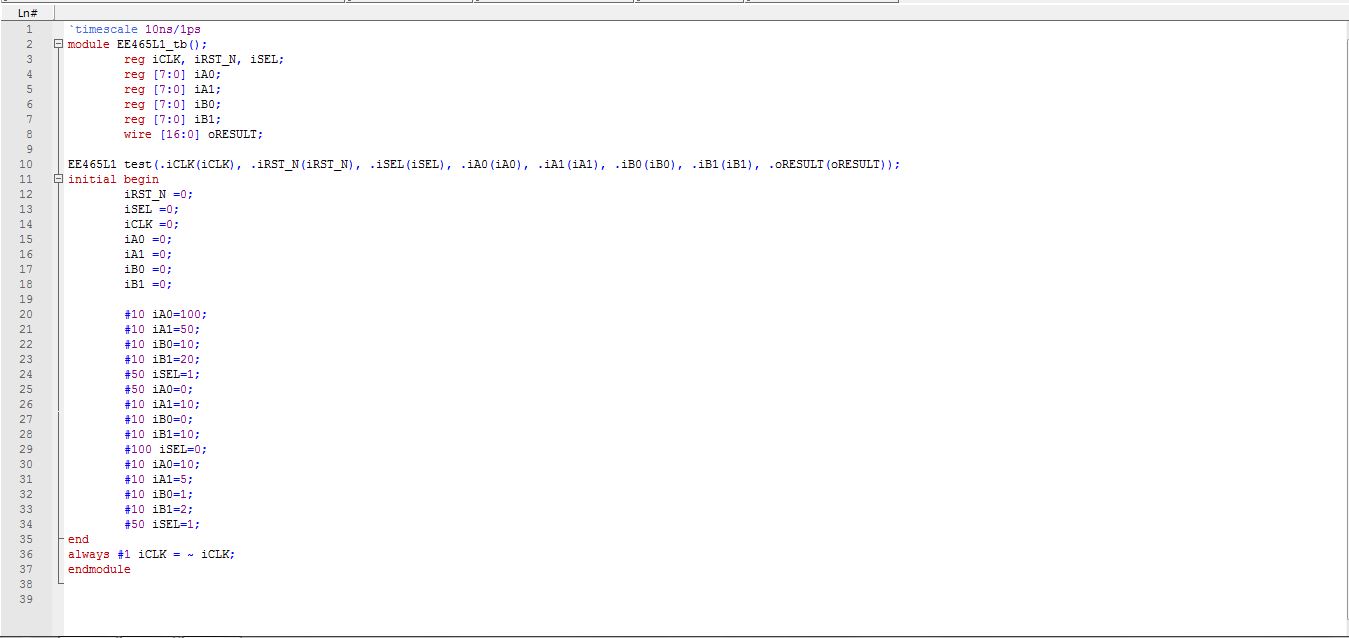


Figure - Test bench Coding.

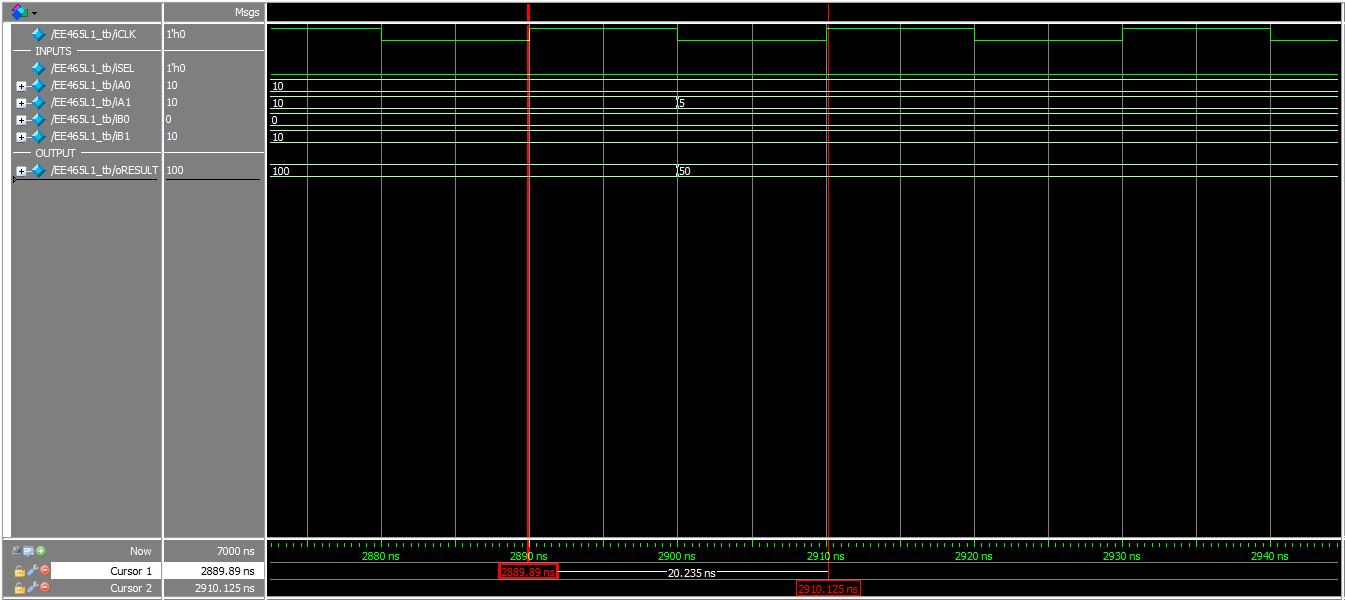


Figure - Period of 20ns or 50MHz clock cycle.

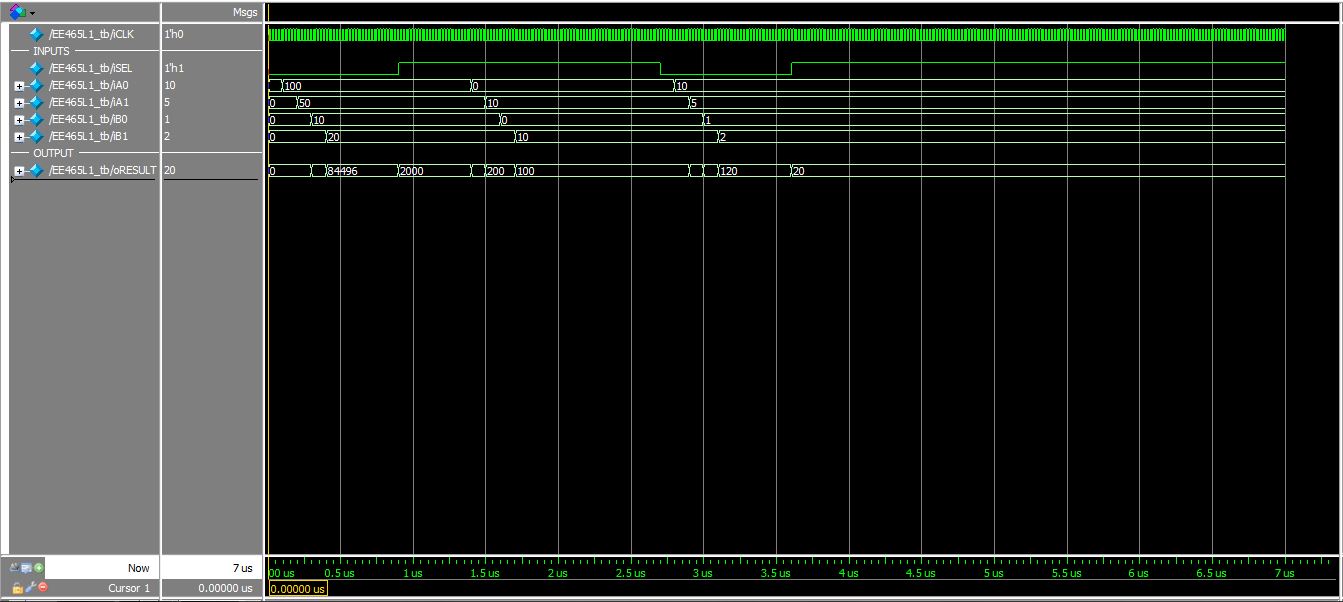


Figure - Full simulation of the lab.

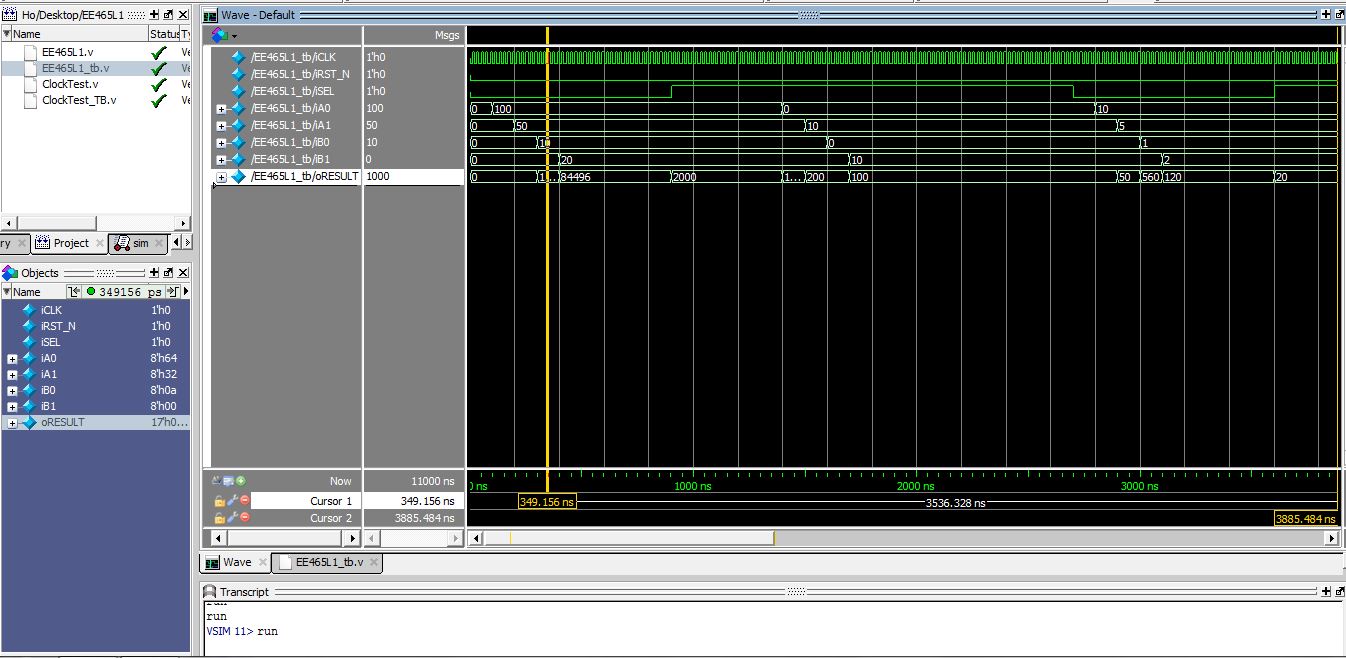


Figure – Comparison of step 3 from the above table. Since the graph is not wide enough to show the oRESULT of 1000.

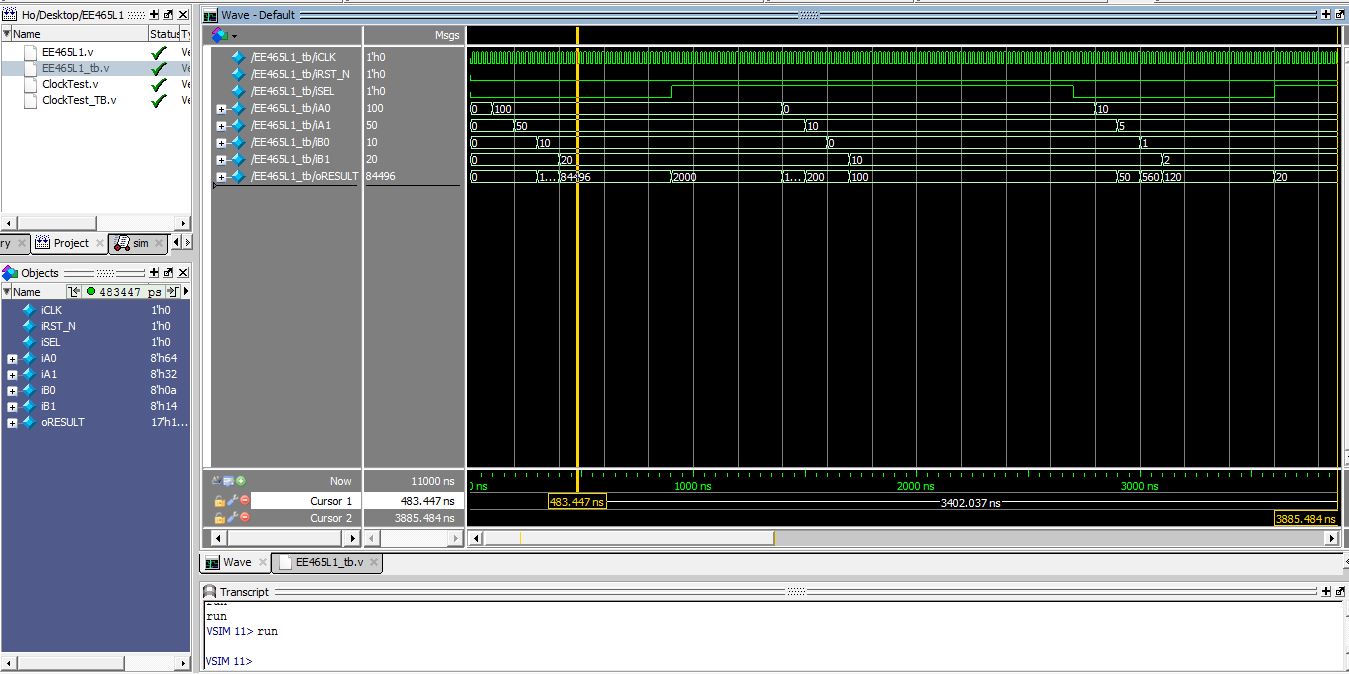


Figure - Comparison on step 4 from the above table shows the overflow of the circuit.

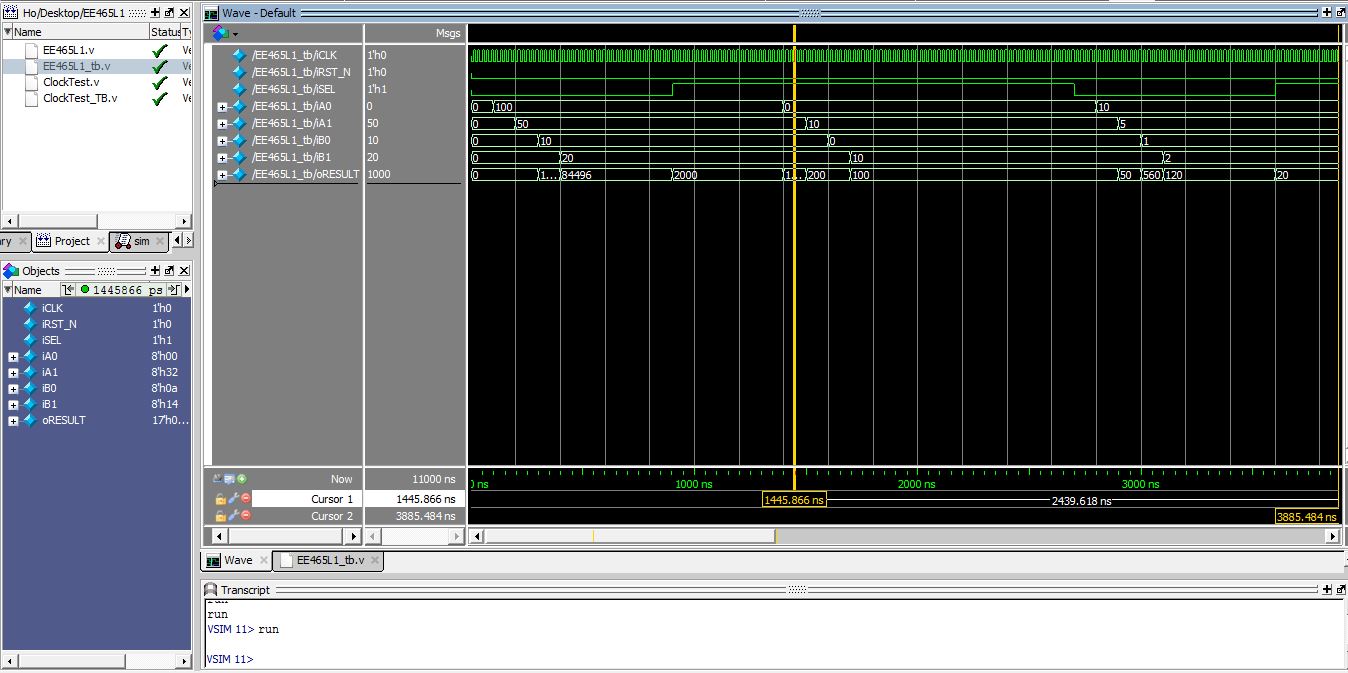


Figure - Comparison of step 9 to the above table, since it is too narrow to see in the graph.

Conclusion

This lab went fairly well for me, the only problem is that i was not able to make during the lab time due to being out of town. It just take a little long to get the clock cycle right to 50MHz or 20nanasecond. As all the figures and calculations from the table above shows that the results are exact with the simulations.